REMARKS

The Office Action mailed on November 16, 2005 as well as the cited art has been reviewed. Claims 1, 2, 4, 5, 7-10, 12, 13, 15-22, 24-26, 28 and 30-34 are pending in this application.

Rejections Under 35 U.S.C. § 103

Claims 1-2, 4-5, and 7-9 were rejected under 35 USC § 103(a) as being unpatentable over Irwin (U.S. Patent No. 6,065,140) in view of Yamamoto et al. (U.S. Patent No. 6,014,414).

Applicant respectfully traverses this rejection.

Claim 1 of the present application is as follows:

1. A phase locked loop, comprising:
a phase comparator having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;
a loop filter having an input for receiving the error signal and an output for providing a control signal;
an oscillator having an input for receiving the control signal and an output for providing a timing signal, wherein the feedback signal is derived from the timing signal;
a processor coupled to the oscillator, wherein the processor is further coupled to receive a status message indicative of a quality level of the reference clock signal; and
a machine-readable medium coupled to the processor, wherein the machine-readable medium has instructions stored thereon capable of causing the processor to monitor the status message and to selectively place the phase locked loop in a holdover condition in response to the status message;
wherein the instructions stored on the machine-readable medium are capable of causing the processor to place the phase locked loop in the holdover condition when a quality level of the reference clock signal indicated by the status message is less than an expected quality level of the phase locked loop in the holdover condition.

The Office Action conceded that Irwin does not explicitly disclose that the PLL of Irwin is placed in holdover when the quality level of the reference clock is below a threshold.

The Office Action took the position that Yamamoto discloses that the "DPLL uses the reference clock signal to place the DPLL in synchronization, using the reference clock signal as a threshold to register when the system is synchronized. . . . The DPLL uses a holdover clock signal if switching to a different reference clock fails. Once the DPLL reaches the holdover reference clock signal, the DPLL is placed in holdover until a new reference clock signal is selected. (Col. 11, lines 4-25)". The Office Action concluded that it would have been obvious to one skilled in the art to incorporate selecting of reference clock signal as disclosed by Yamamoto to Irwin's invention "to effectively provide synchronized clock signals with highest quality level."

It is respectfully submitted that the proposed combination fails to teach or suggest "a machine-readable medium coupled to the processor, wherein the machine-readable medium has instructions stored thereon capable of causing the processor to monitor the status message and to selectively place the phase locked loop in a holdover condition in response to the status message" and "wherein the instructions stored on the machine-readable medium are capable of causing the processor to place the phase locked loop in the holdover condition when a quality level of the reference clock signal indicated by the status message is less than an expected quality level of the phase locked loop in the holdover condition" as recited in claim 1 of the present application.

Yamamoto fails to teach these aspects of claim 1. The DPLL 1912 of Yamamoto is used to *generate* a "holdover clock". In this regard, the Office Action took the position that "[t]he DPLL uses a holdover clock signal if switching to a different reference clock fails. Once the DPLL reaches the holdover reference clock signal, the DPLL is placed in holdover until a new reference clock signal is selected. (Col. 11, lines 4-25)." It is respectfully submitted that the cited portion of the Yamamoto merely describes using the holdover clock generated by DPLL 1912 when a reference clock *fails*.

Nowhere does Yamamoto teach or suggest placing "the phase locked loop in the holdover condition *when a quality level of the reference clock signal indicated by the status message is less than an expected quality level of the phase locked loop in the holdover condition*" as recited in claim 1 of the present application.

Moreover, it is respectfully submitted that one of ordinary skill in the art would not make the proposed combination of Irwin and Yamamoto set forth in the Office Action. Irwin relates to a PLL where a reference signal is generated by a single local crystal or a single local reference oscillator, the output frequency of which can be adjusted (for example, by selecting an integer dividing value R). However, the relevant portions of Yamamoto relied on in the Office Action all relate to synchronization over a network. In Yamamoto, each unit receives multiple synchronization messages and multiple clock references and must select which ones to use for synchronization. See, for example, Yamamoto, column 1, lines 11-13 and column 2, lines 19-36. The Irwin PLL does not receive or otherwise use multiple clock references and therefore has no need to "select" a reference clock from multiple received references in the manner taught in Yamamoto. Instead, the Irwin PLL adjusts the local reference oscillator. Therefore, one of ordinary skill in the art would not be motivated to make the proposed combination.

Claim 2 depends from claim 1 and therefore the arguments set forth above with respect to claim 1 apply to claim 2 as well.

The Office Action rejected claims 4-5 and 7-9 using, in part, similar reasoning as claim 1. Consequently, it is respectfully submitted that the arguments set forth above with respect to claim 1 apply to claims 4-5 and 7-9 as well.

Therefore, it is respectfully submitted that the rejection of claims 1-2, 4-5, and 7-9 be withdrawn.

Claims 10, 12-13 and 15 were rejected under 35 USC § 103(a) as being unpatentable over Irwin (U.S. Patent No. 6,065,140) in view of Yamamoto et al. (U.S. Patent No. 6,014,414), and further in view of Dubberly et al. (U.S. Patent 5,581,555).

Applicant respectfully traverses this rejection.

The Office Action rejected claims 10, 12-13 and 15 using, in part, similar reasoning as claim 1. Consequently, it is respectfully submitted that the arguments set forth above with respect to claim 1 apply to this rejection claims 10, 12-13 and 15. Therefore, it is respectfully submitted that this rejection of claims 10, 12-13 and 15 be withdrawn.

Claim 16 was rejected under 35 USC § 103(a) as being unpatentable over Irwin (U.S. Patent No. 6,065,140) in view of Yamamoto et al. (U.S. Patent No. 6,014,414), and further in view of Dubberly et al. (U.S. Patent 5,581,555), and further in view of Baydar et al. (U.S. Publication No. 2002/0097743).

Applicant respectfully traverses this rejection.

The Office Action rejected claim 16 using, in part, similar reasoning as claim 1. Consequently, it is respectfully submitted that the arguments set forth above with respect to claim 1 apply to this rejection of claim 16. Therefore, it is respectfully submitted that this rejection of claim 16 be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 17, 19-22, 24-25 and 30-32 were rejected under 35 USC § 102(b) as being anticipated by Yamamoto et al. (U.S. Patent No. 6,014,414).

Applicant respectfully traverses this rejection.

Claim 17 is as follows:

17. A method of generating a timing signal, comprising:
generating the timing signal from a reference clock signal in a phase locked loop;
monitoring a status message indicative of a quality level of the reference clock signal; and

placing the phase locked loop in a holdover condition if the quality level indicated by the status message is below a target level;

wherein the method is performed in the order presented.

It is respectfully submitted that Yamamoto fails to teach or suggest" monitoring a status message indicative of a quality level of the reference clock signal" and "placing the phase locked loop in a holdover condition if the quality level indicated by the status message is below a target level" as recited in claim 17 of the present application. In relevant part, the Office Action took the position that Yamamoto discloses "monitoring the status message while selecting the reference clock signal (Col. 5, lines 7-12), placing the PLL in holdover if the holdover reference signal is selected (Col. 5, lines 16-24)." Column 5, lines 7-12 of Yamamoto is as follows:

> The first configuration of the invention allows a clock reference of a high quality level to be selected as the active reference all the time, by entering clock references of a high quality level into the source priority list. Thus, the whole network can be synchronized with a clock of high quality level all the time.

Column 5, lines 16-24 of Yamamoto is as follows:

> Furthermore, by entering a plurality of clock references into the source priority list, sufficient redundancy can be included among the selectable clock references, which circumvents a phenomenon in which the active reference is selected to be the holdover clock or the internal clock, and consequently the whole network is synchronized to a clock of low quality level.

The cited portions of Yamamoto describe trying to *avoid using* the holdover clock but nowhere describes "placing the phase locked loop in a holdover condition if the quality level indicated by the status message is below a target level" as recited in claim 17 of the present application.

Claims 19-21 depend from claim 17 and therefore the arguments set forth above with respect to claim 17 apply to these claims as well.

The Office Action rejected claims 22, 24-25 and 30-32 using similar reasoning as claim 17. Consequently, it is respectfully submitted that the arguments set forth above with respect to claim 17 apply to claims 22, 24-25 and 30-33 as well.

Therefore, it is respectfully submitted that the rejection of claims 17, 19-22, 24-25 and 30-32 be withdrawn.

Claims 26, 28, and 33-34 were rejected under 35 USC § 102(e) as being anticipated by Ogura (U.S. Patent No. 6,542,039).

Applicant respectfully traverses this rejection.

Claim 26 is as follows:

26. (Previously Amended) A method of generating a timing signal, comprising:

during a time when a primary reference clock signal is valid and has an indicated quality level at or above a target level:

generating a first error signal indicative of a phase relationship between the primary reference clock signal and a first feedback signal;

filtering the first error signal to produce a first control signal;

generating the timing signal in response to the first control signal; and

deriving the first feedback signal from the timing signal;

during a time when the primary reference clock signal is failed or has an indicated quality level below the target level, and when a secondary reference clock signal is valid and has an indicated quality level at or above the target level:

generating a second error signal indicative of a phase relationship between the secondary reference clock signal and a second feedback signal;

filtering the second error signal to produce a second control signal;

generating the timing signal in response to the second control signal; and

deriving the second feedback signal from the timing signal; and

during a time when each reference clock signal is failed or has an indicated quality level below the target level:

generating a holdover control signal; and

generating a timing signal in response to the holdover control signal;

wherein the method is performed in the order presented.

Ogura is completely silent as to using a primary reference clock signal and a secondary clock signal as recited in claim 26. The Office Action appears to be taking the position that the "reproduction clock signal" is a second reference clock signal as recited in claim 26. However, Fig. 1 of Osgura clearly shows that the "reproduction clock" is a *feedback signal* and is not a reference clock of any kind. Indeed, the Office Action itself characterizes the reproduction signal as a feedback signal ("deriving a first feedback signal (Fig. 1, label reproduction clock)" Office Action, top of Page 8).

Moreover, the Office Action contains no explanation whatsoever as to how Osgura teaches "generating a holdover control signal" as recited in claim 26 of the present application. The Office Action asserts that "If either of the reference clock signals is below the target level, the PLL is placed in holdover". However, the cited portions of Osgura are completely silent as to placing a PLL in holdover as asserted in the Office Action. Instead, the cited portions relate to how the *feedback signal* (that is, the reproduction clock) is generated (that is, using frequency error or phase error).

The Office Action rejected claims 28 and 33-34 using similar reasoning as claim 26. Consequently, Applicant respectfully submits that the arguments set forth above with respect to claim 26 applies to claims 28 and 33-34.

Therefore, Applicant respectfully requests that the rejection of claims 26, 28, and 33-34 be withdrawn.

CONCLUSION

Applicant respectfully submits that claims 1, 2, 4, 5, 7-10, 12, 13, 15-22, 24-26, 28 and 30-34 are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at 612-332-4720.

Respectfully submitted,

Date: 2 - 16 - 2006

Jon M. Powers
Reg. No. 43,868

Attorneys for Applicant
Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T – (612) 332-4720
F – (612) 332-4731